TECHNICAL DESCRIPTION

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PROJECT NO. 526-207-700619

UNIT DESIGNATION Solid State Super Cascader, Model TML-1[illegible]

General Description

The TML is an all Transistor Main Line Amplifier with high output capability, low noise, low VSWR and gain commensurate for long cascaded systems in the frequency range 54. to 216mc.

The amplifier features a plug-in-pad facility as a course gain control and a vernier gain control for intermediate values. The cable equalizer consists of a 12 and 17 db position and in conjunction with the amplifier tilt control, variable tilt is provided, which ranges from 12 to 23 db of cable.

This amplifier features a temperature compensated current limiting and voltage regulated power supply. The power supply is capable of furnishing -17 VDC at 300 ma to a Jerrold Distribution Amplifier.

The TML incorporates a -17 VDC test point, input RF test point and an RF output test point. Easily available is an input 60 cycle check point on the insulated mounting nut of the power rectifier.

The TML boasts a black solid copper chassis and dust cover for optimum heat transfer. Zener diode biasing is used for ultra stable operation of the power transistors under temperature variations. Gold plated, parallel contacts are used in the cable equalizer to insure long reliable service.

This amplifier may be powered through either RF & AC input fitting or RF & AC output fitting or the Jones Plug with 20 to 30 VAC.

The TML is designed for a nineteen inch rack, cabinet or wall mounting with all controls easily accessible.

Power Supply

Nominal 24 volts AC available from J4, J1 or J7 is rectified by CR3 and filtered by the input filter network C36, R31, R32, C37, then applied to Q1, Q2 and Q3. With collector and bias voltage to Q-1, Q-1 conducts developing output voltage across the bleeder R34, R36, R37, R38 and RT1. R33 allows a stable current flow through CR6 developing

a constant emitter fixed bias to Q3. Common emitter stage Q3 is then turned on by the emitter to base bias developed between the wiper of R36 and ground, minus the voltage across CR6. The dc amplifier Q3 is directly coupled to the base of the emitter follower Q2. The emitter follower Q2 matches the high output impedance of Q3 to the low impedance of the base of Q1. The emitter current of Q2 varies the bias of Q1 allowing it to operate as a variable resistor or as a voltage regulator.

As the load is increased on the power supply the voltage drop across R30 increases. When the R30 voltage drop is that of the fixed bias formed by CR4 and CR5, Q1 is turned off hence current limiting at approximately one ampere.

C40 is used to prevent parasitic high frequency oscillation of Q2 and Q3.

The output voltage is determined by the bias of Q3 which is determined by the setting of R36. The choice of CR6 and the thermistor RT1 is to compensate for variations in transistor Q3's leakage current with temperature.

Equalizers

The components R4, R5, C4, L4, R6, C5, C3, L2, R3 and L3 are used in the 17 db equalizer. R6 and C5 shape the low end of the low frequency response of the equalizer. C4 and L4 shape the high end of the equalizer response. R4, R5 develop the match and R3, L2, L3, and C3 produce a conjugate match at the shaped portions of the extremes of the equalizer response.

The 12 db equalizer composed of R7, R8, R9, R10, C6, C7, C8, L5, L6 and L7 was designed in the same manner as the 17 db equalizer.

RF Circuitry

The RF signals available at either J2 or J1 flow through the equalizer switch and to the PIP socket. The output of the PIP pad flows to the vernier gain control composed of R13, R11 and R12. The 75Ω impedance of the gain control is transformed by T1 to match the input impedance at Q4.

Q4, neutralized by T2 and C13, is a grounded-emitter stage, base-biased by R15 and R29 and emitter-biased by R16. The output impedance of Q4 is transformed by T3 and its response is shaped by L9, R17, R18, R19, C14 and L10 to match the input impedance of Q5.

Q5, a grounded-emitter stage, is zener diode-biased by CR1 for extra stability. Its output impedance is transformed by T4 and shaped by C19 to match the input impedance of Q6. L12, R22, C17, R21 and R20 comprise a variable low frequency feedback network for tilt control.

The output transistor, Q6, is zener diode - biased by CR2 and its output impedance is transformed by T5 to the output fittings J8 or J7. R23, C22 and R24 comprise a low frequency feedback network to acquire a matched 75Ω output impedance for the amplifier.

ALIGNMENT PROCEDURE

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UNIT DESIGNATION Solid State Super Cascader, Model TML-U-1

NOTE: Alignment procedures should be written in a precise, step-by-step outline form. Block diagrams of test set-ups and sketches of scope presentations should be used to clarify the procedure.

1. Equipment Required:

(1) Sweep Generator (JEC 900A/B)
(1) Coaxial Switcher (JEC FD-30)
(3) Attenuators (JEC AV-75)
(1) Oscilloscope (5" w/dc Amplifiers)
(2) Wide Band Amplifiers (JEC SCA-213 or ABC-522)
(1) RF Generator 54 & 216 (JEC CM-6 or CM-10)
(1) Insulated Alignment Tool w/ 1/8" Blade
(1) 405P Power Supply w/4 Prong Jones Plug
(1) Variac (0 to 130 volts)
(1) VSWR Bridge (JEC KSB-75)
(1) Spin Tight 5/16"
(1) Open End Wrench 1/2"
(1) Voltmeter minimum of 1/2% Accuracy (DC)
(1) Dummy Cover
(1) 12 db of Cable at 216 mc (RG-59/U)
(1) 17 db of Cable at 216 mc (RG-59/U)

2. General:

1. J1 & J7 red capped prior to testing.
2. T1, T2, T3, T4 & T5 tinned and solder as close to the ferrite core as possible. Note, the uncomnected splice is positioned away from any connecting terminals and the chassis.
3. RT1 is wired such that its chassis side is wired to the CTC lug which in turn is connected to the chassis ground lug.
4. CR6 is connected with cathode lead aimed toward ground.
5. CR1 and CR2 are connected with cathode side aimed toward dust cover.
6. Adjust R11 maximum clockwise.
7. Adjust R19, 1/4 turn from maximum counter clockwise.
8. Adjust R21 & R36 to maximum clockwise.
9. Adjust C14, C19 & C22 to 1/2 turn from the closed plate position.
10. Position C13 5/16" from the bottom of the screw head to the interstage shield.
11. Q5 and Q6 shall be secured with torque wrench and adjusted for 7 in..lbs.
12. Inspect Power Supply and RF transistor circuitry prior to applying power.

The following procedure shall be used prior to RF Alignment:

Terminate J2 & J8 in 75Ω.
Connect voltmeter to -17 VDC Test Point and Chassis.
Set Variac at minimum.

Slowly bring Variac up to 117 volts to 405P and meter the -17 VDC test point with DC voltmeter (accuracy ± ½%). Once the dc voltage has ceased to change (20 to 30 VAC to Amplifier), set B minus exactly to -17 VDC with R36. Do not allow the test point voltage to exceed -17 VDC. If test point voltage should exceed -17 VDC or power supply does not regulate to -17 VDC shut down immediately and carefully inspect components in power supply.

3. RF Alignment Procedure:

1. Put Equalizer Switch in its thru position.
2. With power on, connect unit for sweep-response using input jack J2 and output jack J8. Rough align amplifier for flat response, using C13, C14, L10, R19, C19 and C22.
3. Terminate J2 and adjust C19 and C22 for output match. Adjust C19 to required output match specification at 216 mc but no further. Adjust C22 for flatness of overall match.
4. Connect unit for sweep response, using input jack J2 and output jack J8. Now adjust C13, C14, L10 and R19 for flatness and gain specs as follows:

(1) C13 peaks at 216 mc only.
(2) C14 & L10 resonate at 216mc. Their L to C ratio determines amplifier tilt.

a) Too much L10 tilts the amplifier response down at the low end.
b) Too little L10 tilts the amplifier response up at the low end.

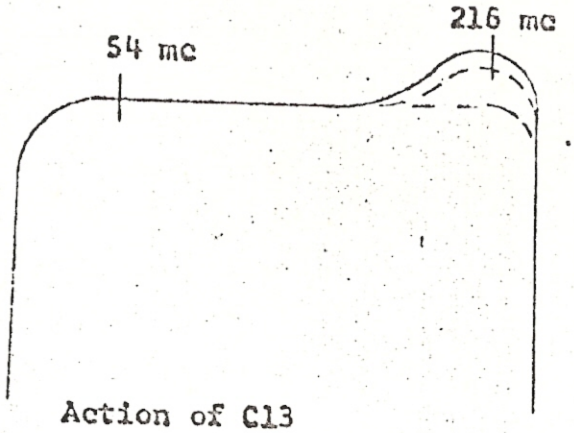
(3) R19 adjusts the roll off at low end of the response.

NOTE:
It may be necessary to adjust C22 slightly to make amplifier flatness specification. This may be done with caution and still hold output match.

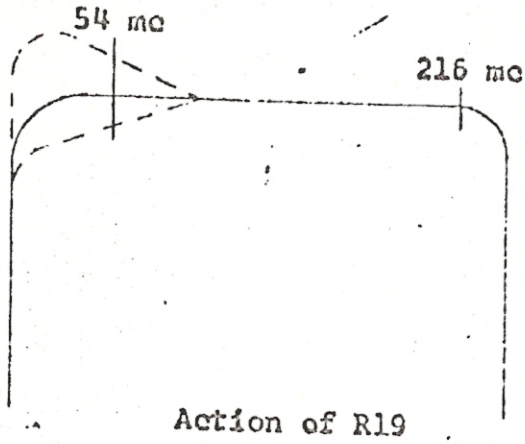
The preceding adjustments will vary as shown in Figure A:

(4) Upon achievement of gain and flatness alignment, recheck output match and check input match.

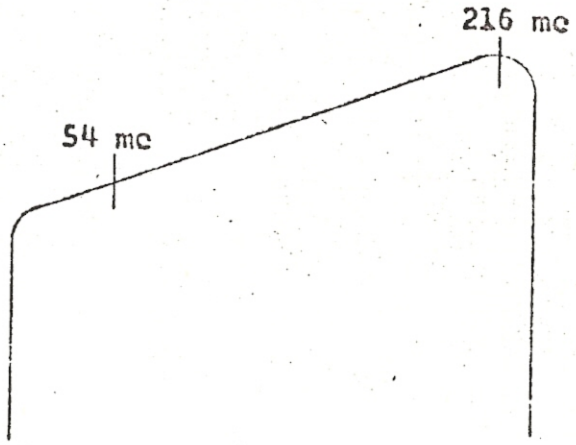
Figure A



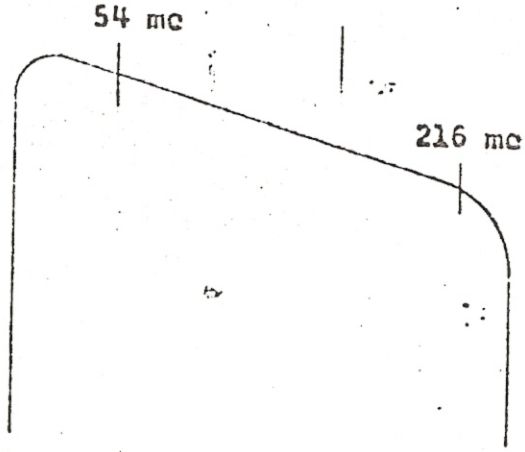
Action of C13



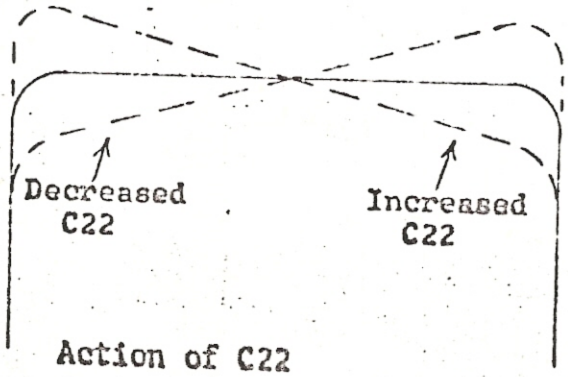
Action of R19



Too much L10 when resonated with C14



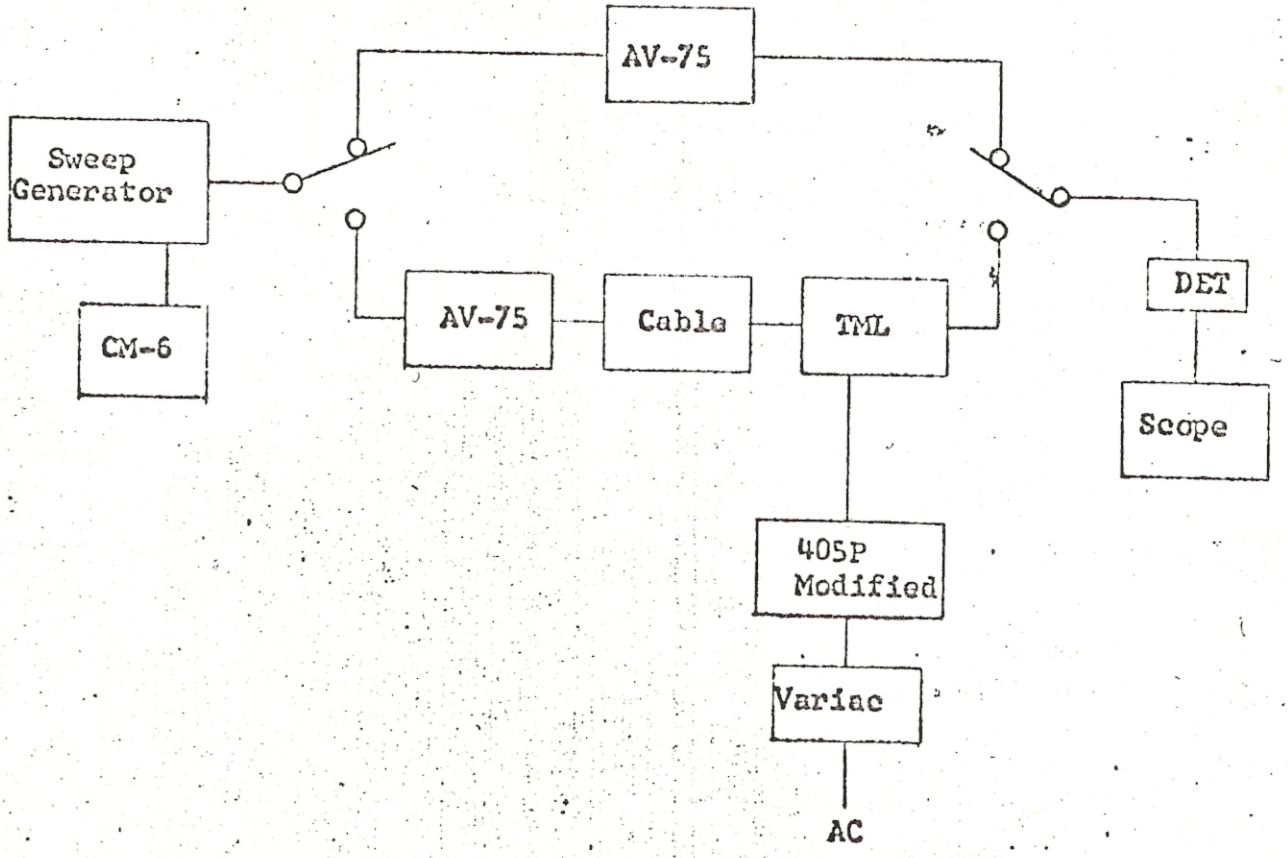
Too little L10 when resonated with C14



Action of C22

5. With 12 db of cable connected to input with normal sweep response, switch cable equalizer to 12 db of cable and adjust L6 & L5 for flatness. L6 will adjust the low end and L5 will adjust the high end.
6. With 17 db of cable connected to input with normal sweep response, switch cable equalizer to 17 db of cable and adjust L3 & L4 for flatness. L3 will adjust the low end and L4 will primarily adjust the high end.

   With 17 db of cable connected to input, switch equalizer switch to 12 db and adjust tilt control for flat response.by adjusting R21 and adjust L12 for flat response.
7. Check input match of amplifier with cable equalizer switch in 12 db & 17 db position.
8. Check action of gain control..
9. Check J5 for -17 VDC at Pin 2 and 20 to 30 VAC at Pin 4, J1 & J7.



AMPLIFIER SPECIFICATIONS

MODEL NO. TTH-1 PROJECT NO. 526-207-700619 DATE 6/10/64

Notes: 1) These are minimum acceptable specifications for production. An Engineering Change Order is necessary when units fail to meet these requirements.
2) Insert "N.A." to mean Not Applicable.
3) Specifications superscripted "3" may be checked on a sample basis unless otherwise indicated.

Band Width 50 to 216 mc

Min. Full Gain 24 db

Flatness ± ¼ db

Skirt Sharpness NA

Gain Control; Type & Performance Plug-In-Pad Facility

3 db Variable

Insertion Loss NA

Tilted Thru Cable _____ db at _____ MC/S; Type Cable See Note 1

Minimum Full Gain Output[3] 42 dbj for 9 Channels

for 0.014 % (-57 db) Cross Mod. See Note 2

Maximum Full Gain Noise Figure [3] 11 db @ Channel 13 & 10 db @ Channel 2

Ripple - (P to P Volts) [3] 5 mv

Impedance At Terminal	Ohms	Bandwidth	Max. VSWR	Min. Ret. Loss, DB
Input	75	54 - 216	1.38:1	16 db
Output	75	54 - 216	1.38:1	16 db

NOTE: 1. Cable Compensation - 12 db fixed with 6 db variable and 17 db fixed with 6 db variable (range 12-23 db of cable)
2. Output capability, 44 dbj for 9 Channels @ -57 db cross mod. for 3 db block tilt.

Form No. 36 Rev. 9/62

AMPLIFIER OPERATIONAL INFORMATION

MODEL NO. TML-1 PROJECT NO. 526-207-700619 DATE 6/10/64

TUBE COMPLEMENT:

RECOMMENDED OPERATING LEVELS WITH TYPICAL CONDITIONS AT THESE LEVELS

GAIN 22 db

INPUT LEVEL + 8 dbj (Highs) + 5 dbj (Lows) *

NOISE FIGURE 14 db (High) 13 db (Lows)

OUTPUT LEVEL 30 dbj (Highs) 27 dbj (Lows)

DISTORTION -87 db Cross Mod. Level

POWER REQUIRE NA ☐ INT. 19 VAC - 30 VAC ** ☒ EXT.

PRIMARY 19-30** VOLTS; 60 CYCLES; .4 AMPS; 12 WATTS

SECONDARY _____ VOLTS _____ M.A.

_____ VOLTS _____ M.A.

_____ VOLTS _____ M.A.

_____ _____

REGULATOR (TYPE) Current Limiting and Voltage Regulating - 17 VDC

*Block Tilt
5 Low Band Chan
4 High Band Cha

MECHANICAL SPECIFICATIONS

HOUSING (Type) Copper

FINISH Black

OVERALL DIMENSIONS 19" Long x 3½" Wide x 2-5/8" Deep

NET WGT. 4½ lbs.

MOUNTING Rack, Wall or Deck (Optional Mtg. Ears)

**NOTE: When used with a TBA-1 or [illegible], the input voltage becomes 21 to 30 VAC.